**VERIFICATION CONTRACT ENGINEER Irvine, CA (6-12 MONTHS)**

**RESPONSIBILITIES:**

We are looking to hire a Verification Engineer with hands-on test experience, excellent communication skills and leadership skills. As a Verification Engineer you’ll help define write the test harness to verify complex FPGAs. You will design and implement test benches, come up with a test plan, write test cases, run test regressions to help verify designs. You may get involved in bring-up and system validation of ASIC & FPGAs.

**BASIC QUALIFICATIONS:**

         Bachelor of Science Degree in computer engineering or electrical engineering.

         3+ years of experience verifying complex ASICs / FPGAs.

         3+ years of experience in ASIC / FPGA verification using C/C++ and/or System Verilog.

         1+ years of experience with verification methodology like OVM / UVM / MM.

         1+ years of experience with building and setting up scalable simulation / verification environments.

         1+ years of experience with scripting (bash/csh, Perl, TCL, Python, etc.).

**PREFERRED SKILLS AND EXPERIENCE:**

         Master’s Degree in Computer Engineering, Electrical Engineering or equivalent.

         Constrained Random Verification Experience, highly desired.

         Any FPGA/ASIC design experience is a definite plus.

         Experience with high reliability design and implementations.

         Experience with any packet based protocols (PCI Express etc.), Network centric designs (Ethernet, IP, FC).

         Familiarity with testing complex designs, code coverage, functional coverage, assertions.

         Ability to focus on finding design issues, corner cases and out of box ideas to make designs more robust.

         Demonstrate the ability to work in a dynamic environment that includes working with changing needs and requirements.